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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/796,480
Filing Date: March 8, 2004
Appellant(s): AVERY et al.

Robert J. Crawford
For Appellants

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 5, 2007 appealing from the Final Office action mailed October 13, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed Upon Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. patent 6,425,101 Garreau July 23, 2002

(9) Grounds of Rejection

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

2. Claims 1-10, 13-14, 16-18, 22-26 and 29 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Garreau (6,425,101).

Claims 1, 4, 6, 8 and 29:

Garreau discloses the invention substantially as claimed. Garreau discloses (figures 2 & 4) a test network (200) including a master controller (202) having a JTAG controller (210) [which represents as recited "test-signal sensing circuit"] connected to a programmable switch (204 or 400) [which represents as "routing circuitry having test signal routing paths with controllable switches"]. The programmable switch (204) is connected to a slave target device (206) [which represents as "a target circuit device] containing JTAG compliant integrated circuits (IC1 through IC4). The master controller (202) further comprises the JTAG controller (210) [represent as "test-signal sensing

circuit"] and a switch controller (218) [which represent as "control logic circuit"] for providing JTAG test protocols by using an I/O line (211-1) and data to the slave target device (206), and receiving the test results by using the feed backward line (211-2) via the programmable switch (204 or 400) (figures 2 & 4, column 4 lines 41-column 5 line 36).

Garreau further teaches (figure 4) that the programmable switches (204 or 400) further comprises combination [represent as "switch-control interface circuit"] of horizontal data line controller (408) and a vertical data line controller (406) which are being controlled by the switch controller (218) [represent as "control logic circuit"] (column 6 line 64-column 7 line 1).

Garreau does not explicitly teach the controllable switches. Garreau, however, teaches (figure 4) that the programmable switch (400) comprises a plurality of vertical data lines (402) being programmably connected to horizontal data lines (404) forming programmable connectors (412). Each programmable connector is located at every horizontal and vertical data line intersect. Each of the horizontal data lines (404) is connected to one of the programmable switch I/O lines (410). Each of the programmable switch I/O lines (410) are in turn connected in a pair-wise manner to the ICs (IC1 through IC4) located on the target hardware device (206) such that each IC can be selectively tested (column 6 lines 60-63; column 6 lines 49-column 7 lines 28).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's programmable connectors (412) formed by connections of plurality of vertical data lines (402) and the plurality of the horizontal data lines (404)

(in Garreau's programmable switch [204]) and such Garreau's programmable connectors (412) would have been the controllable switches. One having ordinary skill the in the art would be motivated to realize so because (a) Garreau teaches that the vertical data lines (402) programmably connected to horizontal data lines (404) forming what is referred to as a "crossbar switch" (column 6 lines 53-56) and (b) Garreau's connections/intersections [of vertical data lines (402) and horizontal data lines (404)] are the crossbar switches (412) which are used for selectively connecting an IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

Claim 2:

Garreau also teaches (figure 7) that a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable switch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 3:

Garreau does not explicitly teach a memory for storing the corresponding configuration data before sending such configuration data to the master controller (704). However, it would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's host computer (702) would have comprised a memory for storing such configuration data. One having ordinary skill in the art would

be motivated to realize so because having a memory for storing (configuration) data inside a computer (or a host computer) is well-known in the art.

Claim 5:

Garreau does not explicitly teach a memory for storing control signals. Garreau, however, teaches that the JTAG controller (210) provides/sends JTAG test protocols (including instructions) used by JTAG test circuitry (figure 2, column 4 lines 60-65).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's JTAG controller (210) would have comprised a memory for storing JTAG test protocols for sending them out to the test circuitry. One having ordinary skill in the art would be motivated to realize so because using a memory to store certain data before sending such data out would have been a matter of design choice and such a choice would not affect the result of the testing on a circuit.

Claim 7:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2) (figure 4, column 8 lines 48-58; column 5 lines 10-36).

Claim 9:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits (IC3 and IC2) can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 8 lines 32-58; column 5 lines 10-36).

Claim 10:

Garreau also teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable switch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 13:

Garreau further teaches that the JTAG controller (210) provides/sends JTAG test protocols including test vectors used by JTAG test circuitry via the I/O line (211-1) (figure 2, column 4 lines 60-65).

Claims 14 & 18:

Claims 14 and 18 are rejected for reasons similar to those set forth against claims (1 & 5) and (2 & 5).

Claim 16

Garreau further teaches (figure 4) that the programmable switch (400), which is controlled by the JTAG controller (210) and the switch controller (218), comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits (IC3 and IC2) can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 8 lines 32-58; column 5 lines 10-36).

Claim 17:

Garreau's master controller (704) directs the programmable switch (706) to selectively couple an IC in responsive to the configuration data from the host computer (702) (figure 7, column 8 lines 62-62).

Claim 22:

Garreau does not explicitly teach an analog-to-digital converter (ADC) (in the configurator arrangement) for converting analog signal to digital signal. It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's test network (200) would have been comprised of an A/D converter. One having ordinary skill in the art would be motivated to realize so because the use of an A/D converter for converting analog data into digital data is well-known in the art.

Claims 23 and 26:

These claims are similar to claims 1-3 except that the feature of monitoring the JTAG I/O test nodes to detect connectivity to another inter-connectable circuit is being recited.

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's JTAG controller (210) would encompass the feature of monitor the JTAG I/O test nodes to detect the connectivity of the ICs. One having ordinary skill in the art would be motivated to realize so because Garreau's JTAG controller (210) is capable of testing only the integrated circuit IC1 after the switch controller (218) directs the programmable switch (204) to connect an I/O line (211-1) to a feed forward line (220) and the feed backward line (222) to an I/O line (211-2) (figure 2, column 5 lines 26-36).

Claims 24-25:

Garreau's configuration data is provided to the master controller (704) which directs the programmable switch (706) to selectively couple the IC (708) to the master controller (704) (figure 7, column 8 line 57-column 9 line 5).

(10) Response to Argument

3. Appellants' arguments filed June 5, 2007 have been fully considered but they are not fully persuasive.

A. The 35 U.S.C. 112/2nd Rejection of claims 1-29:

(i) The appellants' remarks of regarding pending claims 1-29 that being recited with terms including "adapted to", "adaptively" and "adapted for" are persuasive. Therefore, the 35 U.S.C. 112/2nd rejection for claims 1-29 is now withdrawn.

(ii) For claim 9, the appellants' remarks regarding to claim 9 are again persuasive. Therefore, the 35 U.S.C. 112/2nd rejection for claim 9 is now also withdrawn.

B. The 35 U.S.C. 103(a) Rejection of claims 1-10, 13-14, 16-18, 22-26 and 29:

(i) For independent claims (claims 1, 14, 23 and 29), the appellants further argues that Garreau does not teach a test-signal sense circuit that detects the presence of test signals carried by routing paths to control the switching of signals on the paths. The examiner does not agree appellants' remarks.

First, the appellant should aware of the breadth of what is being recited in the claims. The claims recite "a test-signal sense circuit **to** detect test signals... and a control logic circuit **to** send control signals... in response to the detected test signals...." (in claim 1). The use of the preposition "to" (after an element and before a verb) creates "intended use" limitations. In order to meet an intended use limitation all that is required is that the device in question be able to perform the claimed function. Similarly, limitations that employ phrases such as "adapted to", "capable of", "sufficient to", "for" doing something, or "to" doing something are typical of claim limitations which merely recited statements of intended use and may not distinguish over the prior art. With respect to the claims in the instant application, the recitation of the detecting function for the test-signal sense circuit is merely a statement of intended use. In addition, the recitation of the sending function for the control logic circuit also a statement of intended use. As these functions can clearly be met by the test-signal sense circuit and control logic circuit of Garreau, these claim limitations are met Garreau.

Finally, even though the actual detecting and sending functions are recited in statements of intended use, such functions are in fact taught by Garreau. Garreau

teaches the JTAG controller (210) senses or detects test results of an IC (IC1, IC2, IC3 or IC4) that is being feedback from a feed back path (211-2). Garreau also teaches that the ICs can be tested in a priority order. For example, if the IC1 is to be the first integrated circuit to be tested, then when the testing of IC1 has been completed, the process is repeated for all ICs to be tested upon the test protocol executed by the master controller (202) (column 5 lines 22-36, column 6 lines 18-32).

It would have been obvious to one skilled in the art at the time the invention was made to realize that in order for Garreau's master controller (202) to realize when testing of the IC1 has been completed, the JTAG controller (210) [inside the master controller (202)] should perform the feature of sensing the test results from the IC1 already. Such completion of sensing feature [being performed by JTAG controller (210)] would have lead the master controller (202) to send instructions to the switch controller (218) for later activating and testing another IC. One having ordinary skill in the art would be motivated to realize so because when the testing of IC1 has been completed, the process is repeated for all other ICs to be tested upon the test protocol executed by the master controller (202) (column 6 lines 18-32).

Similar limitations in other independent claims (claims 14, 23 and 29) are also rebutted and rejected for above reasons similar to those set forth against claim 1.

(ii) For claims 1, 14, 23 and 29, the appellants also argue that Garreau does not teach nor suggest the "controllable switches". The examiner, however, respectfully traverses the appellant's position. As states in the above 35 U.S.C. 103 rejection for claims 1, 14, 23 and 29 (see ¶2 above), Garreau does teach the programmable connectors (214) (figure 4). Such programmable connectors (214) would have been similar to the "controllable switches". This is because one skilled in the art would be motivated to realize so because (a) Garreau teaches that the vertical data lines (402) programmably connected to horizontal data lines (404) forming what is referred to as a "crossbar switch" (column 6 lines 53-56) and (b) Garreau's connections [of vertical data lines (402) and horizontal data lines (404)] are the crossbar switches (412) which are used for selectively connecting an IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

(iii) For claims 1, 14, 23 and 29, the appellants further argue that Garreau fails to teach controllable switches "for coupling test signals between dedicated test signal circuitry and a target circuit device". Again, as states in the rejection in paragraph 2 above, Garreau's connections [of vertical data lines (402) and horizontal data lines (404)] are the crossbar switches (412) which are used for selectively connecting an IC [in the target device (206)] to JTAG controller (210) via I/O lines (211-1 and 211-2) (figures 2 and 4, column 7 lines 12-28).

(iv) For claims 1, 14, 23 and 29, the appellants allege that Garreau fails to teach "a switch-control interface circuit to control the controllable switches". Well, such limitations are actually taught by Garreau. Garreau does teach (figure 4) that the combination of horizontal data line controller (408) and a vertical data line controller (406). The horizontal data line controller (408) controls certain programmable connectors (412-1 & (412-2) to connect horizontal data lines (402-1) to the vertical data lines (402-1) and the horizontal data line (404-2) to vertical data line (402-2). The vertical data line controller (406) uses the programmable connector (412-3) to connect the vertical data lines (402-1) to the JTAG controller (210) by way of the I/O line (211-1). The vertical data line controller (406) then uses the programmable connector (412-4) to connect the vertical data line (402-2) to the JTAG controller (210) by way of the I/O line (211-2). In this way, a test feedback loop is formed between the JTAG controller (210) and the IC1 in the target device (26) (figure 4, column 7 lines 11-28).

(v) For claim 23, the appellants also allege that neither Garreau's master controller (202) nor the slave target device (206) includes test signals routing switches. The appellants further allege that switching in the Garreau reference is separate from either the master controller (202) or the slave device (206). The examiner, however, respectfully traverses appellants' remarks.

Firstly, the appellants should aware what is being claimed. What is being claimed is "a microcontroller on a first one of ... circuit boards .... automatically configure the ... routing switches (without any specific location) ... on at least the first one of the ...circuit boards". Base on this limitation, since no specific location is being

recited for the routing switches, it is the examiner's position to interpret the routing switches are located on the first one of the circuit board and such a circuit board is also having the microcontroller. In other words, the recited routing switches [are located only on the at least the first one (singular) of the circuit boards] are being recited in the body of the claim. Such routing switches are suggested by Garreau. Garreau teaches the programmable switches (400) having a plurality of programmable connectors (412). Garreau also teaches the master controller (202). Even though the programmable connectors (412) in the programmable switch (400) and the master controller (202) are separated, it would have been obvious to one skilled in the art at the time the invention was made to house both Garreau's programmable switch (400) and Garreau's master controller together and then name such a housing as "(the) first one of the inter-connectable circuit boards". One having ordinary skill in the art would be motivated to realize so because housing two elements (i.e. Garreau's programmable switch [400] and master controller [202]) together and then name such a housing with another name (i.e. "the first one of the inter-connectable circuit boards") would have not affect any performance of the two elements.

(vi) For dependent claims 2-10, 13, 16-18 and 24-26, the appellants states "the section 103(a) rejections of all dependent claims must be reversed in view of the above discussion regarding the independent claim rejections".

The examiner, however, does not agree with the appellants' statement. Since the 35 U.S.C. 103(a) rejection for independent claims (claims 1, 14, 23 and 29) still

stands [see art rejection in ¶2 and rebuttals in ¶3(B)(i)-(v) above], these dependent claims are also still obvious in view of Garreau [see 103(a) rejection in ¶2 above].

C. Motivation for modifying the Garreau reference in the section 103(a) rejection for claims 1-10, 13-14, 16-18, 22-26 and 29.

The appellants further alleges that there is no motivation to realize that Garreau's combination of vertical and horizontal data lines function as controllable switches and therefore the rejection lacks motivation for modifying Garreau reference.

The examiner admitted that this is a typographical error in the Final office action (mail on October 13, 2006) of the word "combination" (in the obviousness statement in the art rejection). Accordingly, the word should have been "connections" instead. The examiner apologizes any inconvenience that occurs to the appellants. The examiner now response to the proper rejection as stated in 35 USC 103 rejection for claim 1 (see 4th paragraph of art rejection for claim 1 in ¶2 above).

In the rejection in claim 1 above, the examiner made the correction and re-stated more clearly as "It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's programmable connectors (412) formed by connections of plurality of vertical data lines (402) and the plurality of the horizontal data lines (404) (in Garreau's programmable switch [204]) and such Garreau's programmable connectors (412) would have been the controllable switches". In other words, it would have been definitely obvious for one skilled in the art to have motivation for modifying such Garreau's "programmable connectors (412) formed by connections"

as the controllable switches. Such motivation would have been (a) Garreau teaches that the vertical data lines (402) programmably connected to horizontal data lines (404) forming what is referred to as a "crossbar switch" (column 6 lines 53-56) and (b) Garreau's connections/intersections [of vertical data lines (402) and horizontal data lines (404)] are the crossbar switches (412) which are used for selectively connecting an IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

D. Correlation between the Garreau reference and each claimed limitation in section 103(a) rejection for claims 1-10, 13-14, 16-18, 22-26 and 29.

Applicant argues that Examiner failed to show or allege correlation between the Garreau reference and the claimed limitations in the manner that accurately conveys the nature of the rejection to the appellants. Upon appellants' request, the section 103(a) rejections are now restated clearly (in ¶2 above) with correlations between the Garreau reference and the claimed limitations.

E. The Provisionally Non-Statutory Obvious-type Double Patenting Rejections of claims 1, 2, 4, 8, 14-17, 23, 26-27 and 29:

According to the combination of remarks from the appellants (as stated on page 12 in the Appeal Brief) and tremendously amended claims in the copending application 10/796,484. The provisionally non-statutory obvious-type double patenting rejections (for claims 1, 2, 4, 8, 14-17, 23, 26-27 and 29) are not longer valid.

Therefore, Such provisionally non-statutory obvious-type double patenting rejections are now withdrawn.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Christine Tu

Conferees:

Guy Lamarre

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